UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/044,242	01/10/2002	Richard D. Taylor	10010391-1	8963

7590 06/18/2004

AGILENT TECHNOLOGIES, INC.
Legal Department, DL429
Intellectual Property Administration
P.O. Box 7599
Loveland, CO 80537-0599

EXAMINER	
ABRAHAM, ESAW T	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 06/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/044,242	TAYLOR ET AL.	
	Examiner	Art Unit	
	Esaw T Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/10/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims **1-24** are presented for examination.

Information Disclosure Statement

2. The examiner has been considered the references listed in the information disclosure statement submitted on 01/10/02.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims **1-4, 9-16 and 22-24,** are rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. (U.S. PN: 5,748,640).

As per claims **1, 11 and 22,** Jiang et al. teach or disclose testing of dynamic random access memories (DRAM), and particularly to a built-in self-test (BIST) for a DRAM array incorporated into a microprocessor such that the built-in self-test can operate in mode while functional tests are being run on the microprocessor core (see col. 1, lines 8-12). Jiang et al. in figure 1 teach a system having a built in RAM (volatile memory) (102) and processor (104), and test unit (105) implemented in one or more machines or microcode wherein the test unit is configured to activate the processor and the RAM (see col. 4, lines 19-31). Jiang et al. **do not explicitly teach** memory checker (memory detector) including a test code configured to detect errors. **However,** Jiang et al. in figure 5 and 6 test began to test a core, built-in self-test begins by the core test bit in the status/control set and if an error detected (see figure 5, step 2008 and figure 6, step 2034) the test will stop (Step 2010) or if no error had been detected then the status bits would be set or reset (see figure 5, steps 2016, 2018 and figure 6, steps 2042, 2046), which Jiang et al.'s system is using similar methods of testing and detecting errors. **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made follow the flow charts of figures 5 and 6 of Jiang et al. to test and check errors of the volatile memory (RAM). **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because providing a memory checker or detector that are detecting faults are well known futures of BIST.

As per claims **2, 3 and 15,** Jiang et al. teach all the subject matter claimed in claims 1 and 11 including Jiang et al. in figure 1 disclose an integrated processor (100) comprising a processor core (104), RAM array (102), BIST (built-in tester) (1000, 1002) and test unit (105) integrated within the integrated processor (see col. 4, lines 19-31). Further, Jiang et al. teach a

processing unit having a CPU, RAM and test unit which may be implemented in either a test unit, which may be implemented in either hardware or software to detect soft or hard errors (see abstract).

As per claim **4,** Jiang et al. teach all the subject matter claimed in claim 1 including Jiang et al. in figures 7-9 teach a timing diagram associated with the built-in testing (see figures 7-9).

As per claim **9,** Jiang et al. teach all the subject matter claimed in claim 1. Jiang et al. **do not explicitly** teach that the memory checker are integrated into a printer controller. **Nevertheless,** as would have been well known to one ordinary skill in the art at the time the invention was made, integrating memory checkers or detectors and a controller are required in order to read and calculate the detecting data (such as CRC) by a controller. **Accordingly,** it would have been obvious to one ordinary skill in the art to integrate a detector and a controller because such integration provides a system to check or verify a data to be valid or not valid.

As per claim **10,** Jiang et al. teach all the subject matter claimed in claim 1 including Jiang et al. teach that the RAM and processor implemented in one or more state machines or microcode (see col. 2, lines 45-49).

As per claims **12, 13 and 16,** Jiang et al. teach all the subject matter claimed in claim 11 including Jiang et al. in figure 5 and 6 test began to test a core, built-in self-test begins by the core test bit in the status/control set and if an error detected (CRC) (see figure 5, step 2008 and figure 6, step 2034) the test will stop (Step 2010) or if no error had been detected then the status bits would be set or reset (see figure 5, steps 2016, 2018 and figure 6, steps 2042, 2046).

As per claim **14,** Jiang et al. teach all the subject matter claimed in claim 11 including

Jiang et al. teach that at least one test of said RAM array comprises initializing said RAM array with a data background (see claim 6).

As per claims **23 and 24,** Jiang et al. teach all the subject matter claimed in claim 22. Jiang et al. **do not teach** magnetic recording on a medium. **However,** magnetic recording is known in the art and common element for most of storage systems or memories. **Therefore,** it would have been obvious to one ordinary skill in the art at the time the invention was made to store information in a storage device or memory is capable of as identified magnetic recording in the claims are obvious and well known with the level of ordinary skill in the art. **One ordinary** skill in the art would have been employed various types of storage devices during testing of the memory device ensuring all types of memories tested.

4. Claims **5-8 and 17-21,** are rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. (U.S. PN: 5,748,640) in view of Quach (U.S. PN: 6,625,749).

As per claims **5 and 17,** Jiang et al. teach all the subject matter claimed in claim 1. Jiang et al. do not explicitly teach a recovery module responsive to the error checker or detector. **However,** Quach in analogous art teaches an error recovery routine is invoked when the processor detects a soft error while operating in the redundant execution mode (see abstract). Further, Quach teach that an error recovery routine is stored in a memory and the recovery routine is accessed when the processor, implementing a program thread in redundant mode, detects a soft error (see col. 3, lines 53-67 and col. 4, lines 1-8). **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to implement the teachings of Jiang et al. to include a recovery module (a program unit or routine)

associated with the error checker or detector. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because a recovery routine (module) provides a mechanism to restore integrity to the execution cores of a processor operating in redundant mode, when discrepancy is detected between results generated by the execution cores (see col. 8, lines 19-22).

As per claims **6, 7 and 21**, Jiang et al. in view of Quach teach all the subject matter claimed in claims 5 and 17 including Quach teaches that the recovery routine initializes the execution cores with the recovered processor state data (see col. 3, lines 63-65). Further, Quach in figure 5A, element 102 teaches a second complete set of processor state data for reinitializing the execution cores of processor (102) (see col. 11, lines 21-23).

As per claim **8,** Jiang et al. in view of Quach teach all the subject matter claimed in claim 5 including Jiang et al. in figure 5 and 6 teach a test began to test a core, built-in self-test begins by the core test bit in the status/control set and if an error detected (see figure 5, step 2008 and figure 6, step 2034) the test will stop (Step 2010) or if no error had been detected then the status bits would be set or reset (see figure 5, steps 2016, 2018 and figure 6, steps 2042, 2046). Further, Quach teaches that in redundant mode, execution cores (110) execute the same instructions from a code segment in lock step, and the results are compared by check unit (CRC) (130) to detect errors in either execution core (110) (see col. 4, last paragraph).

As per claim **18,** Jiang et al. in view of Quach teach all the subject matter claimed in claim 17 including Quach teaches that soft errors arise when alpha particles or cosmic rays strike an integrated circuit and alter the charges stored on the voltage nodes of the circuit (see col. 1, lines 12-32).

As per claim **19,** Jiang et al. in view of Quach teach all the subject matter claimed in claim 17 including Jiang et al. teach a self-tester (BIST) (see figure 1, elements 1000, 1002).

As per claim **20,** Jiang et al. in view of Quach teach all the subject matter claimed in claim 17. Jiang et al. in view of Quach **do not explicitly** teach that the memory checker are integrated into a printer controller. **Nevertheless,** as would have been well known to one ordinary skill in the art at the time the invention was made, integrating memory checkers or detectors and a controller are required in order to read and calculate the detecting data (such as CRC) by a controller. **Accordingly,** it would have been obvious to one ordinary skill in the art to integrate a detector and a controller because such integration provides a system to check or verify a data to be valid or not valid.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 6,085,334 Giles et al.

US PN: 6,415,403 Huang et al.

US PN: 6,560,733 Ochoa

US PN: 4,757,503 Hayes et al.

US PN: 5,619,513 Shaffer et al.

6. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (703) 305-7743. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Esaw Abraham

Esaw Abraham

Art unit: 2133

Gary J. Lamarre
for

Albert DeCady
Primary Examiner